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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/763,859	01/23/2004	Tae Heon Lee	AMKOR-053G	8528
7663	7590	06/30/2005	EXAMINER	
STETINA BRUNDA GARRED & BRUCKER			CAO, PHAT X	
75 ENTERPRISE, SUITE 250				
ALISO VIEJO, CA 92656			ART UNIT	PAPER NUMBER
			2814	
DATE MAILED: 06/30/2005				

Please find below and/or attached an Office communication concerning this application or proceeding.

AK

Office Action Summary

Application No.

10/763,859

Applicant(s)

LEE ET AL.

Examiner

Phat X. Cao

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 07 April 2005.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 12-27 and 32-35 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 12-17 and 32-35 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date <u>5/7/04, 5/10/04</u> . | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

1. The cancellation of claims 1-11 and 28-31 in Paper filed on 4/7/05 is acknowledged.

Priority

2. Acknowledgment is made of applicant's claim for priority under 35 U.S.C. 119(a)-(d) based upon an application filed in Korea on 10/15/1999. A claim for priority under 35 U.S.C. 119(a)-(d) cannot be based on said application, since this United States application was filed on 1/23/2004 which is more than twelve months thereafter. ***Claim***

Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 12-18, 21-25, 27, and 32-35 are rejected under 35 U.S.C. 102(b) as being anticipated by Bayan et al (US. 6,452,255).

Regarding claims 12, 16, 22 and 32, Bayan (Figs. 6A-6F) discloses a method of fabricating a semiconductor package, comprising the steps of: a) providing a lead frame which includes: a die paddle 207 having opposed, generally planar top and bottom surfaces; and a plurality of leads 209 which extend at least partially about the die paddle 207 and each have opposed, generally planar upper and lower lead surfaces and an inner lead end; b) etching the lead frame such that each of the leads includes a half etched portion 240 which is formed in the lower lead surface, extends to the inner lead

end, and defines a generally planar etched lead surface which is disposed in opposed relation to the upper lead surface and extends in generally co-planar relation to the top surface of the die paddle 207 (see Figs. 6B and 6C); c) attaching a semiconductor chip 220 to the top surface of the die paddle 207; d) electrically connecting the semiconductor chip 220 to at least one of the leads 209 by wire bonding 222; and e) at least partially encapsulating the lead frame 209 and the semiconductor chip 220 with an encapsulation material 225 such that at least a portion of the lower lead surface of each of the leads 209 is exposed in the encapsulation material 225 (see Fig. 6F).

Regarding claims 13-15, 23-25 and 33-35, Bayan further discloses that etching the entirety of the top surface of the die paddle 207 and etching a portion 240 of the lower lead surface of each of the leads 209 simultaneously (see Fig. 6B) in amounts sufficient to cause the lead thickness of each of the leads 209 to exceed the paddle thickness 207 and the top surface of the die paddle 207 to extend in generally co-planar relation to the etched lead surface of each of the leads (see Fig. 6C).

Regarding claims 17-18, Bayan's (Fig. 6F) further discloses that the bottom surface of the die paddle 207 and the lower lead surface of each of the leads 209 are exposed from the encapsulation material 225 and extend in generally co-planar relation to each other.

Regarding claims 21-27, Bayan (Fig. 6C) further discloses the step of plating the upper lead surface of at least one of the leads 209 with an electrical conductivity enhancing material 216 (column 6, lines 7-9).

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5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

6. Claims 12-13, 16-18, 22-23 and 32-33 are rejected under 35 U.S.C. 102(e) as being anticipated by Li et al (US. 2004/0217450).

Regarding claims 12, 16, 22 and 32, Li (Figs. 3A-3E) discloses a method of fabricating a semiconductor package, comprising the steps of: a) providing a lead frame 310 which includes: a die paddle having opposed, generally planar top surface 313 and bottom surface 311; and a plurality of leads 312 which extend at least partially about the die paddle and each have opposed, generally planar upper and lower surfaces and inner lead end; b) etching the lead frame 310 such that each of the leads 312 includes a half etched portion which is formed in the lower lead surface (Fig. 3A), extends to the inner lead end, and defines a generally planar etched lead surface which is disposed in opposed relation to the upper lead surface and extends in generally co-planar relation to the top surface 313 of the die paddle (see Fig. 3E); c) attaching a semiconductor chip 320 to the top surface 313 of the die paddle; d) electrically connecting the semiconductor chip 320 to at least one of the leads 312 by wire bonding 330; and e) at least partially encapsulating the lead frame 310 and the semiconductor chip 320 with an

encapsulation material 340 such that at least a portion of the lower lead surface of each of the leads 312 is exposed in the encapsulation material 340.

Regarding claims 13, 23 and 33, Li (Fig. 3A) further discloses that etching the lead frame 310 such that each of the leads 312 has a lead thickness (i.e., 0.2 mm) between the upper and lower lead surfaces thereof which exceeds a paddle thickness (i.e., 0.1 mm) of the die paddle between the top and bottom surfaces thereof.

Regarding claims 17-18, Li (Fig. 3E) further discloses that the bottom surface of the die paddle and the lower lead surface of each of the leads 312 are exposed in the encapsulation material 340 and extend in generally co-planar relation to each other.

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

8. Claims 19 and 26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bayan et al or Li et al in view of Yang (US. 6,730,544).

Neither Bayan nor Li disclose the step of plating the bottom surface of the die paddle and the lower lead surface of each of the leads with a corrosion-minimizing material.

However, Yang (Fig. 7) teaches the step of plating the bottom surface of the die paddle and the lower lead surface 102 of each of the leads with a corrosion-minimizing material (not shown, see column 6, lines 23-26). Accordingly, it would have been

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obvious to plate the bottom surface of the die paddle and the bottom surfaces of the leads of Bayan and Li with a corrosion-minimizing material because such material would protect the exposed bottom surfaces of the die paddle and the leads from the oxidation.

9. Claim 20 is rejected under 35 U.S.C. 103(a) as being unpatentable over Bayan et al or Li et al in view of Glenn et al (US. 6,281,568).

Neither Bayan nor Li disclose the step of exposing a portion of the upper lead surface from the encapsulation material.

However, Glenn (Fig. 6) teaches the step of applying the encapsulation material 55 such that a portion of the upper lead surface of each of the leads 32 is exposed (also see column 10, lines 45-53). Accordingly, it would have been obvious to expose a portion of the upper lead surface of Bayan and Li from the encapsulation material in order to facilitate connection of a solder interconnection to the package, as taught by Glenn (see abstract, second paragraph).


10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Phat X. Cao whose telephone number is (571) 272-1703. The examiner can normally be reached on Monday - Thursday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael Fahmy can be reached on (571) 272-1705. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

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Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

PC
June 24, 2005


PHAT X. CAO
PRIMARY EXAMINER